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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,964	02/19/2004	Christophe Chevallier	400.184US07	4423

7590 12/28/2004

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EXAMINER	
LEVIN, NAUM B	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/781,964	CHEVALLIER ET AL.	
	Examiner	Art Unit	
	Naum B Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/19/04*.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1, 12 and 16 are objected to:

the recitation of "line width parameter" and "actual line width" are not clear to what applicants intend to mean;

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 3-11 are rejected under 35 U.S.C. 102(b) as being unpatentable by Majors (US Patent 5,581,475).

As to claim 1 Majors discloses method for interactively tailoring topography of integrated circuit layout in accordance with electromigration model-based minimum width metal and contact/via rules including:

A method of design rule checking an integrated circuit, comprising (Abstract):

identifying any line (interconnect metal) having a line width marker (layout highlights) and line width parameter (topology parameters/dimensions of interconnect metal/minimum device geometry values Wmin) (col.21,ll.25-39; col.2,ll.52-61; col.10,ll.45-67);

extracting (selecting/deriving) each line having a line width marker (col.11,ll.1-39; col.18,ll.53-67; col.19,ll.1-11);

determining the line width parameter for each extracted line (col.11,ll.40-67; col.12,ll.1-12); and

comparing the line width parameter with an actual line width for the line (col.22,ll.21-43).

As to claims 3-11 Majors recites:

(3) The method of claim 1, and further comprising generating an error condition when the actual line width for the line is less than the line width parameter (col.22, ll.34-56);

(4) The method of claim 1, and further comprising indicating (highlighting error regions) or recording an error (col.22, ll.34-56; col.23, ll.14-35);

when the actual line width for the line is less than the line width parameter.

(5) The method of claim 1, wherein each line having a width marker has a width greater (exceeds minimum width) than a minimum width for that line (col.23, ll.14-35);

(6) The method of claim 1, wherein identifying any line comprises identifying any line in a schematic (col.2, ll.52-61; col.10, ll.45-67);

(7) The method of claim 1, wherein each extracted line has a line width marker in a layout (col.11, ll.1-39);

(8) The method of claim 1, wherein each extracted line has a line width marker in a line width layer (col.10, ll.45-67; col.11, ll.1-39);

(9) The method of claim 1, wherein the line width parameter represents a minimum line width for the line associated with that line width parameter (col.10, ll.45-67);

(10) The method of claim 1, and further comprising extracting a width for each extracted line (col.23, ll.14-35);

(11) The method of claim 1, wherein determining the line width parameter for each extracted line comprises extracting the line width marker and line width parameter for each extracted line (col.11, ll.40-67; col.12, ll.1-12).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2 and 12-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Majors in view of Suzuki (US Patent 5,706,295).

As to claims 12, 16 and 2 Majors discloses:

(12) A method of design rule checking an integrated circuit, comprising (Abstract):

identifying any line (interconnect metal) having a line width marker (layout highlights) and line width parameter (topology parameters/dimensions of interconnect

metal/minimum device geometry values Wmin) (col.21,ll.25-39; col.2,ll.52-61; col.10,ll.45-67);

extracting (selecting/deriving) each line having a line width marker (col.11,ll.1-39; col.18,ll.53-67; col.19,ll.1-11);

determining the line width parameter for each extracted line (col.11,ll.40-67; col.12,ll.1-12); and

comparing the line width parameter with an actual line width for the line (col.22,ll.21-43);

(16) A method of design rule checking an integrated circuit, comprising (Abstract):

identifying any line (interconnect metal) having a line width marker (layout highlights) and line width parameter (topology parameters/dimensions of interconnect metal/minimum device geometry values Wmin) (col.21,ll.25-39; col.2,ll.52-61; col.10,ll.45-67);

extracting (selecting/deriving) each line having a line width marker (col.11,ll.1-39; col.18,ll.53-67; col.19,ll.1-11);

determining the line width parameter for each extracted line (col.11,ll.40-67; col.12,ll.1-12); and

comparing the line width parameter with an actual line width for the line (col.22,ll.21-43).

With respect to claims 12, 16 and 2 Majors teaches the features above but lacks a method of design rule checking an integrated circuit, wherein steps of extracting or comparing exclude lines near or above a transistor.

Suzuki describes a method of checking design rules for semiconductor integrated circuit including:

a method of design rule checking an integrated circuit, wherein steps of extracting or comparing exclude (except) lines near or above a transistor (interconnection data 203 across the specified-region data 801, positioned on the mask pattern data of the transistor that is not included in the region-specified mask pattern data) (Abstract; col.7, ll.64-67; col.8, ll.1-41).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Suzuki's teaching regarding the method of design rule checking an integrated circuit, wherein steps of extracting or comparing exclude (except) lines near or above a transistor and use it in Majors' invention to improve checking of layout line width in IC layouts by decreasing design data value, thereby increasing speed of the IC design verification process.

As to claims 13-15 and 17-19 Majors teaches the features above but lacks a method of design rule checking an integrated circuit, wherein steps of extracting or comparing exclude lines near or above a transistor.

Suzuki describes a method of checking design rules for semiconductor integrated circuit including:

a method of design rule checking an integrated circuit, wherein steps of extracting or comparing exclude (except) lines near or above a transistor (interconnection data 203 across the specified-region data 801, positioned on the mask pattern data of the transistor that is not included in the region-specified mask pattern data) (Abstract; col.7, ll.64-67; col.8, ll.1-41).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Suzuki's teaching regarding the method of design rule checking an integrated circuit, wherein steps of extracting or comparing exclude (except) lines near or above a transistor and use it in Majors' invention to improve checking of layout line width in IC layouts by decreasing design data value, thereby increasing speed of the IC design verification process.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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THUAN DO
Primary examiner
12/23/2004